CLAIMS:

1. An isolation circuit, comprising:

a control circuit to receive as input a power status signal, said control circuit to output a switch control signal, said switch control signal to comprise a switch close signal if said power status is valid, and a switch open signal if said power status is invalid; and

at least one switch to connect to said control circuit, said switch to receive said switch control signal and a component signal and operate in accordance with said switch control signal, with said switch to prevent communication of said component signal when said switch is in an open state.

2. The isolation circuit of claim 1, wherein said control circuit receives as input a software event signal, and said control circuit outputs said control signal in accordance with said software event signal.

3. The isolation circuit of claim 1, wherein said switch receives as input a software control signal, and said switch switches between said open state and a closed state in accordance with said software control signal.

4. The isolation circuit of claim 1, further comprising a plurality of switches, each switch to connect to said control circuit, said plurality of switches to each receive said switch control signal and a component signal and operate in accordance with said switch

control signal, with said plurality of switches to prevent communication of said component signals when said switch is in an open state.

5. The isolation circuit of claim 1, wherein said control circuit receives power from a power supply, and when said control circuit fails to receive said power said control circuit drives said switch to an open state.

6. The isolation circuit of claim 1, wherein said control circuit and said switch comprise at least one N-channel MOSFET.

7. A system, comprising:

a bus;

a shelf having a plurality of shelf components;

a management module to connect to said bus, said management module to manage a plurality of signals communicated between said shelf components; and

wherein said management module comprises an isolation circuit to isolate said signals if one of said shelf components becomes inoperative.

8. The system of claim 7, wherein said isolation circuit comprises:

a control circuit to receive as input a power status signal, said control circuit to output a control signal, said control signal to comprise a switch close signal if said power status is valid, and a switch open signal if said power status is invalid; and

at least one switch to connect to said control circuit, said switch to receive said control signal and at least one of said shelf component signals and operate in accordance with said control signal, with said switch to prevent communication of said shelf component signal when said switch is in an open state.

9. The system of claim 7, wherein said control circuit receives power from a power supply, and when said control circuit fails to receive said power said control circuit drives said switch to an open state.

10. The system of claim 7, wherein said control circuit receives as input a software event signal, and said control circuit outputs said control signal in accordance with said software event signal.

11. The system of claim 7, wherein said switch receives as input a software control signal, and said switch switches between said open state and a closed state in accordance with said software control signal.

12. A circuit comprising:

a plurality of switches, with each switch configured to receive a component signal;

a control circuit to electrically couple to said plurality of switches, said control circuit to comprise a dual N-channel MOSFET to receive a power status signal;

wherein a first MOSFET is turned on and a second MOSFET is turned off when said power status signal is a TTL logic high, and to source current to each switch to allow said component signal to be communicated to an external module; and

wherein said first MOSFET is turned off and said second MOSFET is turned on when said power status signal is a TTL logic low, and to remove said current from each switch to isolate said component signals from said external modules.

13. The circuit of claim 12, wherein each switch comprises a dual N-channel MOSFET configured to default to an off state when power is removed.

14. The circuit of claim 12, wherein each switch may be turned on or off by a software control signal.

15. A method to isolate a signal, comprising:

receiving a power status signal at a control circuit;

receiving a component signal at a switch; and

isolating said component signal at said switch in accordance with said power status signal.

16. The method of claim 15, wherein said isolating comprises:

closing said switch to allow said component signal to be communicated to an external module if said power status signal is valid; and

opening said switch to prevent said component signal from being communicated to said external module if said power status is invalid.

17. The method of claim 16, wherein said closing comprises:

receiving said power status signal indicating a TTL logic high at said control circuit; and

sending current to close said switch.

18. The method of claim 16, wherein said opening comprises:

receiving said power status signal indicating a TTL logic low at said control circuit; and

removing current to open said switch.

19. The method of claim 15, wherein said isolating comprises:

receiving a software event signal from an application program at said control circuit; and

opening said switch to prevent said component signal from being communicated to an external module in accordance with said software event signal.

20. The method of claim 15, wherein said isolating comprises:

receiving a software control signal from an application program at said switch; and

opening said switch to prevent said component signal from being communicated to an external module in accordance with said software control signal.